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Cascaded H-Bridge Eleven Level Inverter With Reduced Number of Switches

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Abstract: In this paper, a new topology of multilevel inverter with reduced number of switches using fuzzy logic controller is proposed to improve the inverter performance. The analysis has been done by sinusoidal pulse width modulation technique. Both conduction and switching losses decrease, the number of switches reduce which leads to increase the inverter efficiency. The size and power consumption of driving circuits are also reduced. Therefore, the overall cost and circuit complexity are greatly reduced. Also, it does not face voltage-balancing problems due to fixed dc voltage values. A simulation in the MATLAB/SIMULINK platform has validated the proposed idea.

Keywords: Multilevel Inverter, Cascaded H-bridge Multilevel Inverter, Total Harmonic Distortion, SPWM, MATLAB

1. INTRODUCTION

In recent years various industrial applications need high power devices [1].Power-electronic inverters are becoming popular for numerous industrial drives applications [2]. A multilevel inverter is a power electronic system that combines and produces a desired output voltage from number of levels of dc voltages as inputs. Recently, multilevel power conversion technology has been improving the power electronics area very rapidly with high potential for further improvements. As a result, the most attractive applications are using medium to high voltage ranges by this technology [3]. A multilevel converter achieves high power ratings and also enables the renewable energy sources usage. For a high power application the renewable energy sources can be easily interfaced to a multilevel converter system.

The multilevel converters have smaller output voltage step, which results in lower harmonic components, high voltage capability , lower switching losses, better electromagnetic compatibility, and high power quality. So smaller output voltage step is taken as advantage of multilevel inverter [1], [4].Also it can be operated at both fundamental and high switching frequency PWM. It should be noted that lower switching frequency usually leads to lower switching loss and higher efficiency [5].

The results of this study search give that circuits of multilevel inverter have been around for more than 25 years. Today, medium voltage levels with high-power applications use multilevel inverters widely [6]. The field applications include use in pumps, laminators,

compressors, conveyors, fans, blowers, and mills. Moreover, several multilevel converter topologies have been developed [3], [7]. Three proposed topologies for multilevel inverters are cascaded multi cell with separate dc sources,capacitor-clamped (flying capacitors) and diode clamped (neutral-clamped) [1]. Each of these topologies has a different mechanism for producing the voltage level. The first topology introduced was the series H-bridge design but many configurations have been obtained for this topology as well [7]. Since this topology consists of series power conversion cells, the levels of voltage and power may be scaled easily. The H-bridge topology was followed by the diode-clamped converter that used a series capacitors banks [8]. The flying capacitor topology followed diode-clamped after few years. Instead of series connected capacitors, this topology uses floating capacitors to clamp the voltage levels [9]. H-bridge inverters have isolation transformers to isolate the voltage source but they do not need either clamping diode or flying capacitor inverters.

In addition to, existing modulation techniques and control paradigms have been created for multilevel converters such as selective harmonic elimination (SHE-PWM),sinusoidal pulse width modulation (SPWM), space vector modulation (SVM), and others [10], [11]. Further, many multilevel converter applications give attention on industrial medium-voltage motor drives [12], utility interface for renewable energy systems [13], traction drive systems and flexible AC transmission system (FACTS) [14], [15].

One clear disadvantage of multilevel power conversion is the more power semiconductor switches needed. One more disadvantage of multilevel power converters is that the small voltage steps are typically created by isolated voltage sources or a series capacitor banks. Isolated voltage sources may not always be readily available and series capacitor banks require voltage balance [16]. Although low-voltage-rated switches can be utilized in a multilevel converter, each switch needs a related gate driver and protection circuits. This may lead the overall system to be more complex and expensive[17].So, in practical implementation, decrease the number of switches and gate driver circuits is very important [18].

In this Paper, a new topology of cascaded h-bridge multilevel inverter has been investigated to increase levels with a low switches and gate driver circuits for generating all levels at the output, without adding any complexity to the power circuit. Finally, simulation results validate the accuracy of the proposed multilevel inverter

2. CONVENTIONAL CASCADED H-BRIDGE MULTILEVEL INVERTER

The single-phase structure of single-phase eleven-level conventional cascaded h-bridge multilevel inverter is illustrated in Figure.1. Every dc source is connected to a single-phase full-bridge, or H-bridge, inverter separately. Every inverter level able to generate three +Vdc, 0 and –Vdc different voltage outputs. The different voltage levels are produced by connecting the dc source to the ac output by switching combinations of the four semiconductor switches Q1,Q2,Q3 and Q4. To obtain +Vdc, switches Q1 and Q2 are tuned on ,whereas –Vdc can be obtained by tuning on switches Q3 and Q4, By turning on Q1 and Q3 or Q2 and Q4, the output

voltage is 0, The ac outputs of each of the full-bridge inverter levels are connected in series such that the combined voltage waveform is the sum of the output of the inverter [19],[20].

The m number of output phase voltage levels in a cascaded inverter is given by m = 2s+1, where s is the number of separate dc sources. Every H-bridge unit generates a quasi-square waveform by phase-shifting the turn on and off timings of its both phase legs (positive and negative).

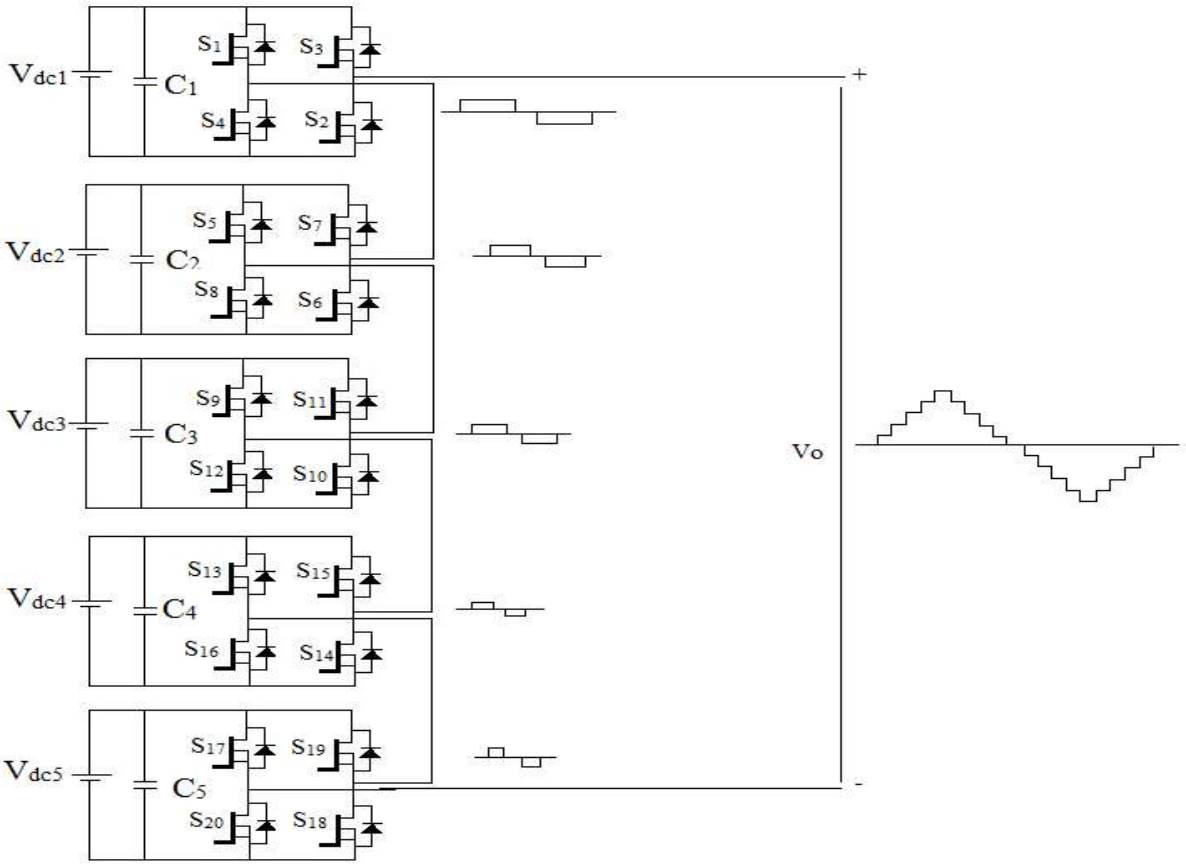

Figure.1 Single phase structure of the conventional cascaded eleven level inverter

3. PROPOSED CASCADED MULTILEVEL INVERTER TOPOLOGY

In conventional cascaded multilevel inverters, the power semiconductor switches are combined together to produce a negative and positive polarity high-frequency waveform. However, there is no necessary to use all the switches for generating two levels. The proposed topology uses this technique.

This topology uses two parts to generate the output voltage. One part is named level generation part and is responsible for different voltage levels generation. The switches in this

part should have high-switching-frequency capability to generate the required levels. The another part is called polarity generation part and is responsible for generating the polarity of the output voltage. This polarity generation part operates at low-frequency (line frequency).The proposed topology combines the high frequency voltage generation and low frequency polarity generation part to generate the output voltage in multilevel. To generate a complete multilevel output, the positive levels generated from the high-frequency level generation part is fed to a polarity generation part (full-bridge cascaded inverter), which will generate the desired output polarity. This will reduce the semiconductor switches which were responsible to generate the positive and negative polarity output voltage levels in conventional cascaded multilevel inverter. The single phase structure of the proposed eleven level inverter topology is shown in Figure. 2. It requires nine switches and five isolated dc sources. The method of this topology is that the left circuit generates the desired output levels (without polarity) and the right circuit cascaded Inverter (full-bridge inverter) decides about the polarity of the output voltage. According to the desired output polarity, the polarity generation part transfers the required output level to the output with the same direction or opposite direction. This topology easily implemented to higher voltage levels by adding additional end stage in level generation part in Figure.2. Therefore, this topology is modular and can be easily increased to higher voltage levels. This topology is also suitable for applications, such as photovoltaic (PV) generators, batteries and fuel cells where separate dc voltage sources are available. The phase output voltage is generated by the sum of the output voltages of every stage, and subsequently will create an elven level output phase voltage.

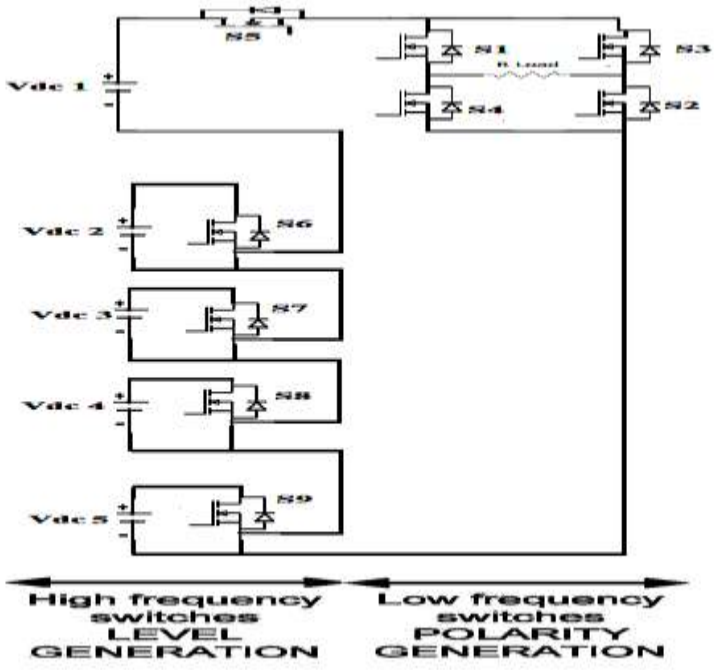

Figure.2.Single phase structure of the proposed multilevel inverter

4. SINUSOIDAL PULSE WIDTH MODULATION

PWM technique is widely used to eliminate low-order harmonics which is harmful in inverters. In PWM control, output voltage is controlled by varying the pulse width. The pulse width variations are by the several times the turned ON and turned off of the inverter switches during a half cycle . The most commonly used is the sinusoidal PWM technique out of the available modulation strategies developed for multilevel inverters.

In sinusoidal PWM instead of maintaining the all pulses width the same as in the case of multiple PWM, the width of each is varied in proportion to the amplitude of a sine wave evaluated at the same pulse. The distortion is reduced significantly compared to multiple PWM. The gating pulses are shown in figure 3.

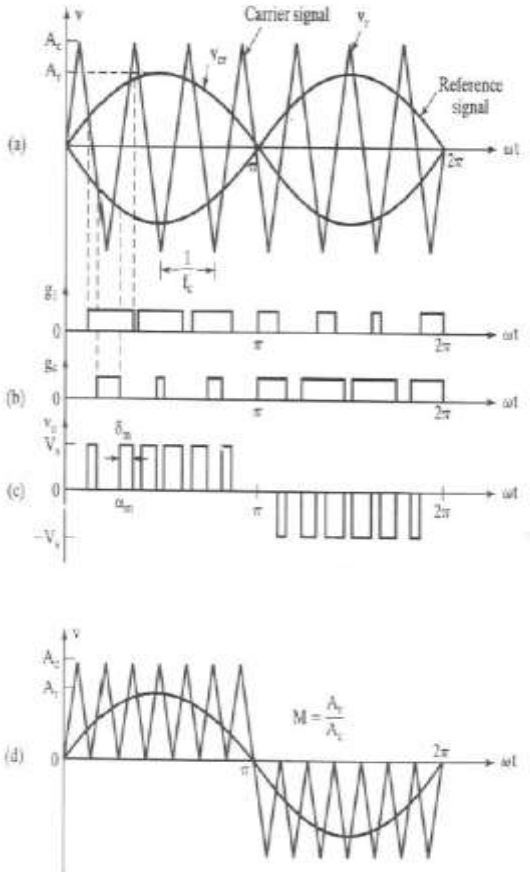

Figure .3 Sinusoidal Pulse width modulation

5. FUZZY CONTROLLER

Fuzzy logic control is developed in this work to obtain desired output voltage and minimize the harmonics of the inverter used. The control action is determined in a FLC by a set

of simple linguistic rules. The rules are determined by the whole process which is to be controlled. A rule-based fuzzy logic controller is used to track the reference voltage for any load condition. The inputs for the fuzzy logic controller are error and rate of change in error. The controller and the inverter of the system are completely built in Matlab / Simulink environment. The fuzzy logic controller consists of three basic blocks. i) Fuzzifier
ii) Inference Engine iii) Defuzzifier.

5. 1.Fuzzifier

The fuzzy logic controller requires that each control variables which define the control surface be expressed in fuzzy set notations using linguistic labels. Five classes of linguistic labels ((Positive Big) PB, (Positive Small) PS, (Zero) ZE, (Negative Big) NB, (Negative Small) NS) characterized by membership grade are used to decompose each system variable into fuzzy regions. The membership grade denotes the extent to which a variable belongs to a particular class/label.

This process of converting input/output variable to linguistic labels is termed as fuzzification. It is implemented using reference fuzzy sets shown in Fig. 4 and used to create a fuzzy set that semantically represents the concept associated with the label. In the proposed controller, the error in voltage e = (Vre, - Vo) and its rate of change are normalized, fuzzified, and expressed as fuzzy sets.

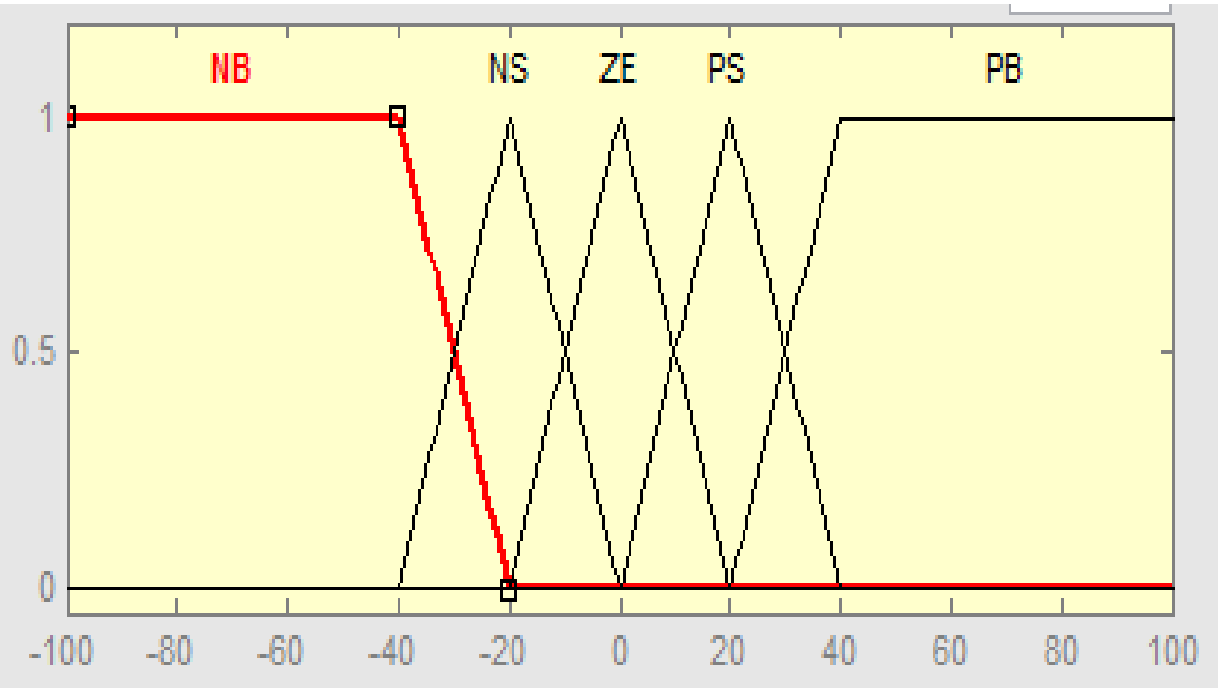

Figure.4. Fuzzy reference sets

Table 1. Rule base of FLC developed for cascaded MLI

Error/Rate of change in error		RATE OF CHANGE OF ERROR				
		PB	PS	ZE	NB	NS
ERROR	PB	PB	PB	PS	ZE	PS
	PS	PB	PS	PS	NS	ZE
	ZE	PS	PS	ZE	NS	NS
	NB	ZE	NS	NS	NB	NB
	NS	PS	ZE	NS	NB	NS

5. 2 Inference Engine

The behavior of the control surface which relates the input and output variables of the system is governed by a set of rules. The set of rules for the fuzzy controller is shown in Table I, which proposes a definite control action for a given error e and its rate of change error. When a set of input variables are read, each of the rule that has any degree of truth (a nonzero value of membership grade) in its premises is fired and contributes to the forming of the control surface by appropriately modifying it. When all the rules are fired, the resulting control surface is expressed as a fuzzy set (using linguistic labels characterized by membership grades) to represent the controller's output.

5.3 Defuzzifier

The defuzzifier is used to achieve the crisp variable, which is used for driving the actuator, of the fuzzy set representing the controller output in linguistic labels . The most commonly used method for the control applications in defuzzification process is Centre of Area method and it is used here. The Centre of Area method computes the centre of gravity of the final fuzzy space (control surface) and produces a result which is sensitive to all the rules executed. Hence, the results tend to move smoothly across the control surface.

6. SIMULATION RESULTS

For verifying the validity of the proposed multilevel inverter in the generation of a desired output voltage waveform, a prototype model is simulated based on the proposed topology according to that one shown in Figure. 2. The Matlab/ Simulink power block set is used for simulation. The fuzzy algorithm is developed and simulated wave forms of output voltage, current and THD are shown.

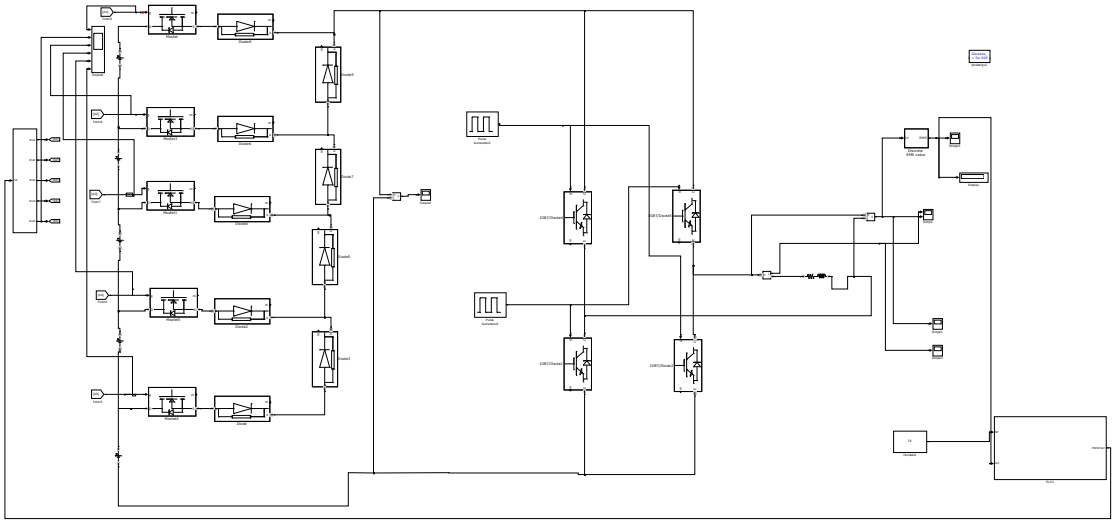

Figure.5. Simulation model of proposed cascaded h-bridge eleven level inverter topology

The simulation model of cascaded h-bridge eleven level inverter topology using SHEPWM is shown in figure.5. The power circuit consists of five H-bridges whose nominal dc voltage is considered to be 24 V and the eleven level stepped output voltage is obtained and the harmonics are reduced. Also it consists of PWM generator block which has parameters as amplitude, pulse width period and phase delay which is used to determine the shape of the output .Therefore the efficiency of the inverter is increased. The inverter should operate reliably and efficiently for supplying a wide range of alternative current loads with the voltage and desired power quality essential for reliable and efficient load and performance of the system. The advantages of the system are high power high voltage capacity, low harmonics and switching loss. The eleven level output voltage and output current can be achieved by using SPWM technique. The output eleven level inverter fundamental frequency is 50 Hz. The loads are connected across the cascaded H-bridge eleven level inverter. The Output voltage and current waveform of Cascaded h-bridge eleven level inverter are shown in figure. 6 & 7.

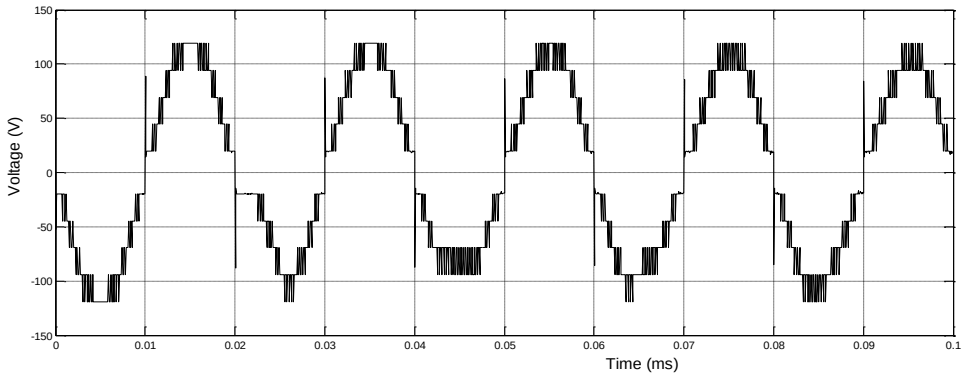

Figure.6. Output voltage waveform of Cascaded h-bridge eleven level inverter

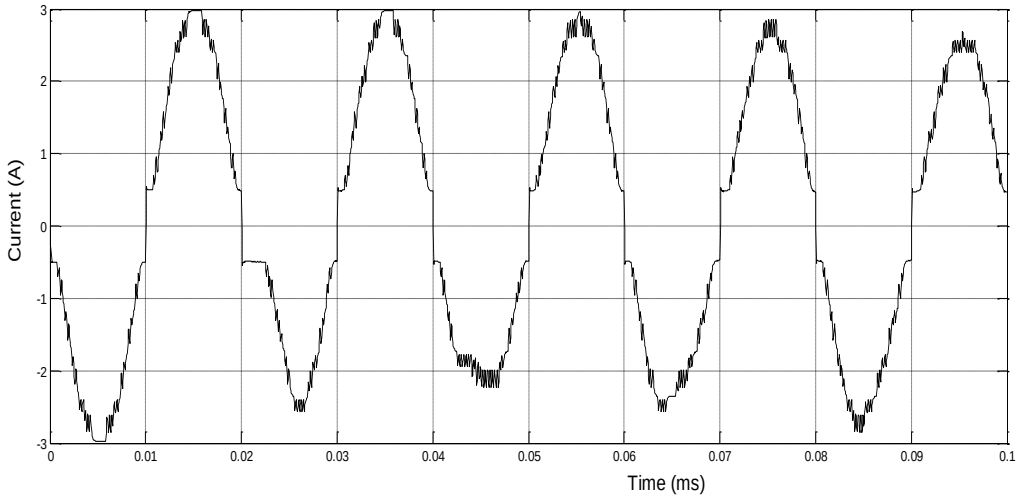

Figure.7. Output current waveform of Cascaded h-bridge eleven level inverter

THD is the summation of all the voltage and current waveform harmonic components. THD is used to illustrate the linearity of audio systems and the power quality of electric power systems. The number of harmonics to be eliminated is equal to the number of switching angles are obtained. The harmonic spectrum of the inverter output voltage is shown in shown in figure.8.

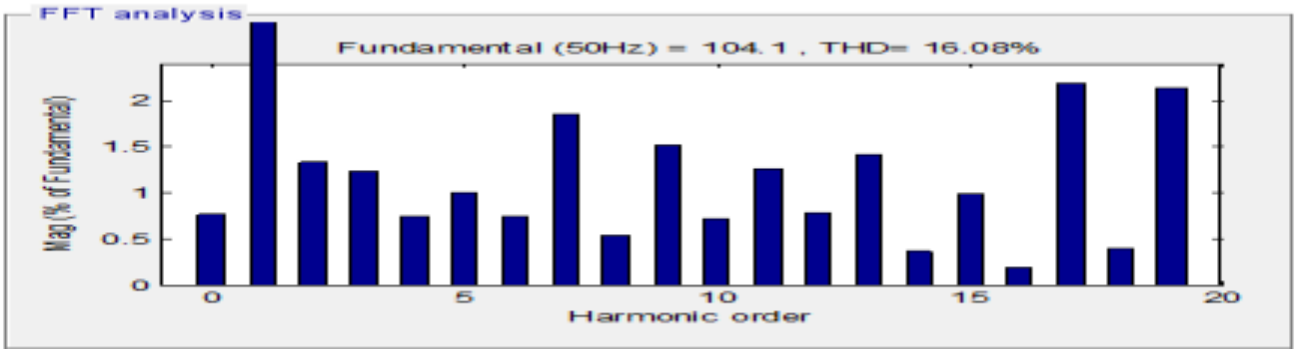

Figure.8. Harmonic spectrum of the inverter output voltage

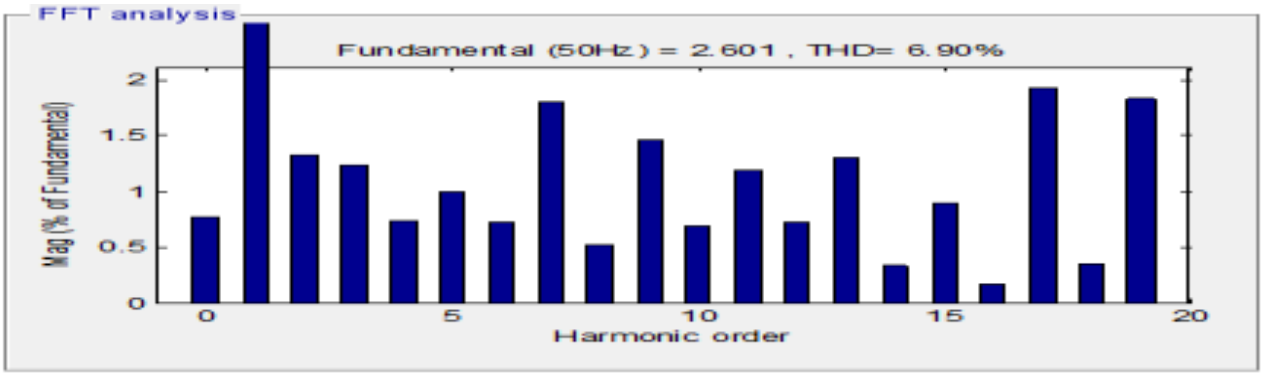

Figure.9. Harmonic spectrum of the inverter output current

7. CONCLUSION

Reduced switch cascaded h-bridge eleven level inverter topology has been proposed in this paper. The main features are less number of required power switches, lower switching losses and cost of the inverter over conventional cascaded multilevel inverter. The switching operation is separated into high-frequency and low-frequency parts. This will increases the inverter efficiency, size of the circuit and cost of the experimental setup. The operating performance of the inverter was found to be better when the fuzzy controller has been used. The simulation results are provided for an eleven level cascaded H-bridge inverter to prove the computational results accuracy.

REFERENCES

[1] J. Rodriguez, J. S. Lai and F. Z. Peng, "Multilevel inverters: Survey of topologies, controls, and applications," IEEE Trans. Ind. Applicat., vol. 49, no. 4, pp. 724-738, Aug. 2002.

[2] Beser, E.; Camur, S.; Arifoglu, B.; Beser, E.K. , " Design and application of a novel structure and topology for multilevel inverter," in Proc. IEEE SPEEDAM, Tenerife, Spain, 2008, pp. 969 – 974.

[3] R.H. Baker, "High-Voltage Converter Circuit," U.S. Patent Number 4,203,151, May 1980.

[4] S. Mekhilef and M. N. Abdul Kadir "Voltage control of three-stage hybrid multilevel inverter using vector transformation" IEEE Trans. Power Electron.,vol.25,no.10,pp 2599-2606, Oct. 2010.

[5] L.M. Tolbert, F. Z. Peng, T. G. Habetler, "Multilevel PWM Methods at Low Modulation Indices," IEEE Trans. Power Electron.,vol. 15, no. 4, pp. 719-725, July 2000.

[6] M. N. A. Kadir S. Mekhilef, and H. W. Ping "Voltage vector control of a hybrid three-stage eighteen- level inverter by vector decomposition" IET Trans. Power Electron.,vol.3,no. 4, pp.601- 611, 2010.

[7] E. Babaei, M. T. Haque, and S. H. Hosseini, "A novel structure for multilevel converters," in Proc. ICEMS, 2005, vol. 2, pp. 1278–1283.

[8] A.Nabae, I. Takahashi, and H. Akagi, "A new neutral-point clamped PWM inverter," IEEE Trans. Ind. Applicat., vol. IA-17, no. 5, pp. 518– 523, Sep./Oct 1981 .

[9] T. A. Meynard and H. Foch, "Multi-level conversion: High voltage choppers and voltage-source inverters," in Proc. IEEE PESC, Toledo , Spain 1992, pp. 397– 403.

[10] S. Mekhilef and M. N. Abdul Kadir "Novel vector control method for three-stage hybrid cascaded multilevel inverter" IEEE Transactions on Industrial Electronics, DOI: 10.1109/TIE.2010.2049716 (in press), 2010, vol. 58, no.4,pp.1339-1349.

[11] S. Mekhilef, A. M. Omar and N. A. Rahim, "Modelling of three-phase uniform symetrical sampling digital PWM for power converter" IEEE Trans. Ind. Electron.,vol. 54, no. 1, pp.427-432, Feb. 2007.

[12] M. F. Aiello, P. W. Hammond, and M. Rastogi, "Modular Multi-Level Adjustable Supply with Parallel Connected Active Inputs," U.S. Patent 6 301 130,Oct. 2001.

[13] L. M. Tolbert, F. Z. Peng, "Multilevel converters as a utility interface for renewable energy systems," in Proc. IEEE Power Eng. Soc. Summer Meeting 2000 ,vol. 2 , pp. 1271-1274

[14] L. M. Tolbert, F. Z. Peng, T. G. Habetler, "Multilevel Inverters for Electric Vehicle Applications," IEEE Workshop on Power Electronics in Transportation, Dearborn, Michigan , 1998, , pp. 1424-1431.

[15] M.N.Abdul Kadir S.Mekhilef and H.W.Ping "Dual vector control strategy for a three – stage hybrid cascaded multilevel inverter," Journal of power Electronic ,vol.10, no.2,pp.155-164,2010.

[16] Najafi, E.; Yatim, A.; Samosir, A.S.; "A new topology –Reversing Voltage (RV) - for multi level inverters, " in Proc. IEEE 2nd International, PECon 2008, pp. 604 – 608.

[17] Babaei E. "A cascade multilevel converter topology with reduced number of switches," IEEE Trans. Power Electron.,vol.23,no.6,pp 2657- 2664,Nov.2008 .

[18] M.E.Ahmed, S.Mekhilef, "Design and implementation of a multilevel three-Phase inverter with less switches and low output voltage distortion," Journal of Power Electronics, vol.9, no.4, pp.593–603, Jul. 2009.

[19] Fang.Z. Peng, John W.Mckeever, and Donald J.Adams, "A Power line conditioner using Cascade Multilevel Inverters for Distribution systems" IEEE Transactions on Industrial Applications, vol. 34, n.6, pp 1293-1298, Nov/Dec 1998. al and Power Engineering, vol. 1, n. 1, Jan 2010, pp 36-40.

[20]B.P.Mcgrath, D.G.Holmes, "Multicarrier PWM strategies for multilevel inverters," IEEE Trans. Ind.Electron, vol 49, n.4, pp 858-867,Aug.2002